

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ON SEMICONDUCTOR CORP. and)
SEMICONDUCTOR COMPONENTS)
INDUSTRIES, L.L.C.,)
Plaintiffs,)

v.)

SAMSUNG ELECTRONICS CO., LTD.,)
SAMSUNG ELECTRONICS AMERICA, INC.,)
SAMSUNG TELECOMMUNICATIONS)
AMERICA GENERAL, L.L.C.,)
SAMSUNG SEMICONDUCTOR, INC., and)
SAMSUNG AUSTIN SEMICONDUCTOR L.L.C.,)
Defendants.)

C.A. No. 07-449 (JJF)

**REDACTED PUBLIC
VERSION**

SAMSUNG ELECTRONICS CO., LTD.,)
SAMSUNG ELECTRONICS AMERICA, INC.,)
SAMSUNG TELECOMMUNICATIONS)
AMERICA GENERAL, L.L.C.,)
SAMSUNG SEMICONDUCTOR, INC., and)
SAMSUNG AUSTIN SEMICONDUCTOR L.L.C.,)
Plaintiffs,)

v.)

ON SEMICONDUCTOR CORP. and)
SEMICONDUCTOR COMPONENTS)
INDUSTRIES, L.L.C.,)
Defendants.)

C.A. No. 06-720 (JJF)

**DECLARATION OF MARTIN G. WALKER, Ph.D. IN SUPPORT OF
ON SEMICONDUCTOR'S OPENING BRIEF IN SUPPORT OF ITS
MOTION TO COMPEL DISCOVERY CONCERNING INFRINGEMENT**

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August 15, 2008
Redacted Filing Date: August 22, 2008

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MOTION TO COMPEL DISCOVERY CONCERNING INFRINGEMENT**

I, Martin G. Walker, Ph.D., declare as follows:

1. I have been retained as an expert consultant by the law firm of Jones Day, counsel of record for ON Semiconductor in the above-captioned matters. This declaration is based on

my personal knowledge and experience as well as my investigation in this matter and reflects my expert opinions on certain issues.

2. My CV (Exhibit A) contains an overview of my thirty years of experience in the field of Electronic Design Automation (“EDA”) software systems. I received a BSEE from the Massachusetts Institute of Technology in 1973, and MSEE from Stanford University in 1976, and a PhD. in electrical engineering from Stanford University in 1979. My work experience includes direct work with EDA software, both as a developer and as a designer, and semiconductor fabrication technology and processes, including electroplating.

3. From 1983 to 1989, I was the founder and Chief Technical Officer at Analog Design Tools, Inc. (“Analog”). In my work at Analog, I was a founder and founding CEO. I was primarily responsible for writing the original business plan and raising the venture capital necessary to launch the company and recruiting the staff. Later, I was responsible for all technical aspects of product definition and development. My efforts were instrumental in growing Analog from a start-up company to a leader in the field of analog design automation.

4. From 1990 to 1994, I was a founder and Executive Vice President of Symmetry Design System (“Symmetry”), which specialized in product design and consulting for the electronic design marketplace. In this role, I was instrumental in development of Symmetry’s products.

5. In 1995, I founded a company called Frequency Technology (now Sequence Design) (“Sequence”) that develops EDA software for the design of advance system-on-a-chip integrated circuits. Sequence’s products have become the de facto industry standard for parasitic extraction, circuit optimization, and RTL power analysis. As Chief Executive Office, director,

and Chief Scientist at Sequence, I was involved in overseeing the development of the company's products and technologies. I also took an active role in recruiting the technical and business staff.

6. Early in my career, I personally used an electroplating machine and processes to create circuits that were incorporated in my Ph.D. research.

7. While at Sequence, I was responsible for developing detailed models of integrated circuit metallization structures, including the dual damascene plated copper structures at issue in the present litigation. Developing accurate models required that I gain a detailed understanding of the electroplating process used to create the structures. Thus, I became, and still am, familiar with the electroplating technology at issue in the present litigation.

8. It is my experience that the semiconductor manufacturer (or "fab") makes a set of design rules for each process.

9. It is my understanding that Samsung employs the L18, L13, L9, L6 and L45 processes to build logic devices. For each of these processes, there is a corresponding set of design rules.

10. Among other things, design rules include specification of the minimum and maximum trench widths, line widths, the height of the trenches, spacing between the trenches, and additional information relating to the geometry and structure of the pads.

11. In my experience, this information is always created by the semiconductor manufacturer or fab so that designers may create designs to be built by the fab using the referenced process.

12. In general, I am familiar with electroplating processes. When you plate substrate features (such as trenches, vias, or pads, for example) with certain geometries, you get non-planar accumulation. For instance, Exhibit B [REDACTED]

[REDACTED]

[REDACTED]

13. Further, Exhibit C is a Samsung document. I've examined Exhibit C at

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

14. Thus, the design rules are relevant to determining the extent to which the above documents are representative of Samsung's logic processes.

I DECLARE UNDER PENALTY OF PERJURY that the foregoing is true and correct.

Executed on August 15, 2008, in Palo Alto, California.

A handwritten signature in cursive script, appearing to read "Martin G. Walker", written in black ink on a white background.

Martin G. Walker

EXHIBIT A

Martin G. Walker, Ph.D.

Curriculum Vitae

Professional Summary

Dr. Walker has over 25 years experience in electronic design automation (EDA) software systems, circuit simulation and circuit design. He is a recognized expert in the field of EDA systems, simulation, and modeling. He also has considerable experience in web applications development and management of high availability web-based systems.

Employment History

From: 2001 **Brass Rat Group, Inc.**
To: Current Woodside, CA
Position: *CEO*

Brass Rat Group is a successful Silicon Valley based consulting organization specializing in litigation consulting and business consulting in the electronic design automation (EDA) field. Dr. Walker has also been engaged in source-code copying litigation, offering opinions in patent, copyright, and trade secret aspects.

From: 2000 **Knowledge Networks**
To: 2001 Menlo Park, CA
Position: *Chief Technology Officer*

Knowledge Networks is a pre-IPO market research company that is leveraging internet technology to revolutionize the market research industry. KN recruited a panel of over 50,000 consumers to be interviewed on a variety of topics weekly. Dr. Walker managed KN's engineering group, which designed and created automated systems to create surveys, conduct interviews, process data, and manage the panel. He also managed the IT group which was responsible for high-availability web-based systems for fielding the interviews as well as the internal systems required to analyze the data and produce real-time reports.

From: 1995 **Sequence Design (Formerly Frequency Technology)**
To: 2000
Position: *Founder, Founding CEO, Director & CTO*

Sequence Design, formerly Frequency Technology, is the leader in the EDA segment called Design Closure. Sequence's products and services, consisting of pre- and post-layout optimization based on accurate layout extraction, enable designers to bring higher performance, lower-power integrated circuits quickly to tape out. Dr. Walker:

- Developed business plan and raised over \$9MM in financing;
- Hired staff and led development, including defining technical product definition;
- Personally developed many of the basic algorithms, which resulted in

Martin G. Walker, Ph.D.
Curriculum Vitae

- five issued patents;
- Led initial marketing efforts;
- Wrote numerous technical articles advancing the company's technical position;
- Served as chief technical spokesman for the company.

From: 1990 **Symmetry Design Systems**

To: 1995 Los Altos, CA

Position: *Founder, Director & Executive Vice President*

Symmetry, a self-funding enterprise, was a service and product business specializing in the analog simulation EDA market. Products included simulation-model libraries, modeling tools, and special-purpose analog simulators. Dr Walker was responsible for a joint venture in Beijing China, where new products were developed. Symmetry was acquired by Analogy, Inc.

- Initiated Japanese and European marketing activities.
- Developed conceptual framework and user-interface model for the Sun OpenLook-based product.
- Served as technical spokesman in customer and industry forums.
- Conducted sales training in the US, Asia, and Europe.

From: 1983 **Analog Design Tools**

To: 1990 Sunnyvale, CA

Position: *Founder, Director, Founding CEO & Chief Scientist*

ADT's first product, the Analog WorkBench, pioneered the market for Analog CAE workstations, including such fundamental concepts as multiple window CAE systems, and simulated test instruments as a paradigm for CAE user interface. ADT, which had grown to \$16MM in annual sales and 150 employees, was acquired by Cadence.

- Formulated original business plan and presented concept to venture investors. Raised initial venture financing. Led fund-raising activities through the series C round.
- Served as President during formative stage. Director and Chief Scientist (CTO) from the founding through acquisition. Set the product direction. Drove the technology development.
- Formulated ADT's initial marketing strategy. The international distribution strategy focused primarily on Japan.
- Developed the Japanese market for ADT's products. Responsible for establishing and maintaining our distributor relationship, negotiating contracts, supporting customers, and building sales that amounted to 20% of the installed base.

Martin G. Walker, Ph.D. Curriculum Vitae

From: 1980 **COMSAT**
 To: 1983 Palo Alto, CA
 Position: *Director, Microwave Systems*
 Managed a Navy sponsored program to develop high productivity techniques for manufacturing of microwave components. Developed a microwave circuit-synthesis product.

From: 1973 **Watkins-Johnson**
 To: 1980 Palo Alto, CA
 Position: *Member of the Technical Staff*
 Developed GaAsMESFET-based microwave amplifiers, components, and tuners. Designed and produced the world's first GaAsMESFET amplifiers to be delivered in production quantities.

Consulting History (within last 5 years)

From: 2005 **Sequence Design**
 To: Current Santa Clara
 Duties: EDA software analysis

From: 2005 **Sabio Labs**
 To: 2005 Palo Alto, CA
 Duties: Create business plan, operating plan, and marketing plan for EDA startup focused on analog circuit optimization and synthesis

Litigation Support Experience

Dr. Walker has testified in a jury trial involving technology software issues and in an arbitration. Dr. Walker also has significant experience in giving deposition testimony and in crafting declarations and expert reports. Dr. Walker regularly works with attorneys to help articulate and manage the many technology issues that arise in complex litigation.

Date: 2000-02 **Thelen Reid (for Plaintiff)**
 Case Sequence Design vs various defendants
 Project: Patent infringement relating to EDA software (I am an inventor of the patents at issue). Provided support for claim construction and infringement analyses.
 Status: Settled

Date: 2001-03 **Dechert, LLP (for Plaintiff)**
 Case Silvaco v Antonau (CSI)
 Project: Misappropriation of trade secrets, including copied source code. Analysis of source code. Worked directly with attorneys and plaintiff; provided numerous declarations that supported this description. Testified at

Martin G. Walker, Ph.D. Curriculum Vitae

		deposition regarding source code copying, other trade secret misappropriation, and business practices.
Status:		Judgment entered against CSI, other claims settled on terms favorable to plaintiff
Date:	2001-02	FTI Teklicon (for IRS)
Case		IRS vs taxpayer
Project:		Analysis of valuation for tax purposes of EDA software and associated royalty streams.
Status:		Completed
Date:	2001-02	Dechert LLP (for Plaintiff)
Case		Synopsys vs Nassda (patent infringement – '053)
Project:		Declaration, expert report, and deposition in support of claim construction. Declaration in opposition to Summary Judgment motion for non-infringement that was denied by the Court. Infringement analysis and expert report. Opposition to invalidity claims.
Status:		Settled
Date:	2001-04	Dechert, LLP (for Plaintiff)
Case		Synopsys vs Nassda (State Action)
Project:		Identification of misappropriated trade secrets. Analysis of source code creation rates. Analysis of electronic evidence tampering. Assist with discovery issues. Manage electronic discovery of more than 300Gbytes of documents. Analysis and declarations regarding disk wiping and other evidence tampering by defendants.
Status:		Settled
Date:	2001	Law offices of Al Reynaldo (for cross-defendant Après)
Case		Aprés vs Ho
Project:		Misappropriation of EDA-related trade secrets. Testified at trial.
Status:		Settled
Date:	2003-04	Dechert LLP (for Plaintiff)
Case		Synopsys vs Nassda (patent infringement – '998)
Project:		Claim construction analysis and declaration. There were 11 disputed terms. The Court adopted Dr. Walker's construction on all 11 terms, rejecting all of the defendants arguments.
Status:		Settled
Date:	2003-04	Dechert LLP (for Respondent)
Case		CSI vs Silvaco
Project:		Arbitration resulting from alleged violation of the terms of the settlement agreement. Testified for two days regarding the CSI's licensing, support and maintenance of certain Silvaco trade secrets.

Martin G. Walker, Ph.D. Curriculum Vitae

Status:	Arbitration completed	
Date:	2003-04	Dechert LLP (for Plaintiff)
Case	HCL vs eKomas	
Project:	Analysis and identification of directly copied source code. The product at issue is a web-based application for loan management.	
Status:	Settled	
Date:	2004	McDermott (for Defendant)
Case	Tera Systems vs InTime Software	
Project:	Patent infringement related to EDA software. Researched invalidity and supported claim construction.	
Status:	Settled	
Date:	2004-05	Dechert LLP (for Plaintiff)
Case	Silvaco vs CSI – OSC re Contemp	
Project:	Analysis and declaration regarding the Defendants' continued use of Silvaco trade secrets.	
Status:	Completed	
Date:	2004-05	Dechert LLP (for Defendant)
Case	Siliconix vs AATI	
Project:	Patent infringement regarding method for manufacturing a semiconductor device. Support for claim construction and invalidity analysis. Researched prior art.	
Status:	Settled	
Date:	2005	Kirkland & Ellis LLP (for Defendant)
Case	Berry vs Fleming, et al.	
Project:	Source code copyright and misappropriation of trade secrets. Reviewed source code at issue. Expert report and declarations in support of summary judgment.	
Status:	Ongoing	
Date:	2005	Dechert LLP (for Plaintiff)
Case	Synopsys vs Magma	
Project:	Patent infringement regarding method EDA software. Support for claim construction and invalidity analysis. Supported source code analysis.	
Status:	Ongoing	
Date:	2005	Browne & Woods LLP (for Defendant)
Case	Keywords vs ISE	
Project:	Investigated allegations of source code copying and copyright infringement. Declaration ISO of opposition to preliminary injunction.	
Status:	Settled	

Martin G. Walker, Ph.D. Curriculum Vitae

Date:	2005	Jones, Day (for Plaintiff)
	Case	Experian v. I-Centrix
	Project:	Investigating allegations of source code copying and misappropriation of trade secrets.
	Status:	Ongoing
Date:	2005	Dechert LLP (for Plaintiff)
	Case	Silvaco vs CSI End Users
	Project:	Analysis and declarations regarding the Defendants' continued use of Silvaco trade secrets.
	Status:	Ongoing
Date:	2005	DLA Piper (for Defendant)
	Case	Hynex v. Toshiba
	Project:	Patent infringement investigations (invalidity, claim construction, non-infringement) relating to EDA patent.
	Status:	Ongoing

Patents

<u>Patent Number</u>	<u>Date Issued</u>	<u>Title</u>
6,643,831	2003	Method and system for extraction of parasitic interconnect impedance including inductance
6,381,730	2002	Method and system for extraction of parasitic interconnect impedance including inductance
5,901,063	1999	System and method for extracting parasitic impedance from an integrated circuit layout

Education

<u>Year</u>	<u>College/University</u>	<u>Degree</u>
1987	AEA/Stanford Executive Institute	Completed w/distinction
1979	Stanford University, Stanford, CA	Ph.D., Electrical Engineering
1976	Stanford University, Stanford, CA	MS, Electrical Engineering
1973	Massachusetts Institute of Technology, Boston, MA	BS, Electrical Engineering

Publications

Over fifty articles in the fields circuit design and design automation, including technical papers in peer-reviewed journals, an invited article in the IEEE Spectrum, and various conference proceedings. I have organized seminars, which were designed to enhance the technical credibility of my companies, and written numerous opinion pieces published in journals such as EETimes that served to establish and promote our corporate position.

Martin G. Walker, Ph.D.
Curriculum Vitae

Professional Associations and Achievements

- 1999 Fortune Magazine "Cool Company" for Frequency Technology.
 - 1984 Electronic Products New Product of the Year award for the Analog Workbench
 - 1976 IEEE Microwave Applications award recognizing contributions to the design of GaAsFET amplifiers.
-

**EXHIBIT B –
FILED UNDER SEAL**

CONFIDENTIAL EXHIBIT

**EXHIBIT C –
FILED UNDER SEAL**

CONFIDENTIAL EXHIBIT

CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on August 22, 2008, I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Josy W. Ingersoll
John W. Shaw
Andrew A. Lundgren

I also certify that copies were caused to be served on August 22, 2008 upon the following in the manner indicated:

BY HAND AND EMAIL

Josy W. Ingersoll
John W. Shaw
Andrew A. Lundgren
YOUNG, CONAWAY, STARGATT & TAYLOR LLP
The Brandywine Building
1000 West Street, 17th Flr.
Wilmington, DE 19899

BY EMAIL

John M. Desmarais
James E. Marina
KIRKLAND & ELLIS
153 East 53rd Street
New York, NY 10022

/s/ Richard J. Bauer

Richard J. Bauer (#4828)